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Configuring Current Sharing on the ZL2004 and ZL2006

Introduction

This application note describes the features and setup procedure for the ZL2004 and ZL2006 devices configured in current sharing groups. These products employ an inter-device communication Bus called the Digital-DC bus (DDC bus). The DDC bus enables Zilker Labs IC's to exchange critical real-time telemetry to any device connected to the Bus. The DDC bus enables advanced power management, fault management, sequencing, and many other features not available in the previous generation of products.

Overview

A current sharing group is simply 2 or more parallel converters operating at the same frequency, but interleaved in such a way to multiply the input and output ripple frequency by the number of paralleled converters or phases. Paralleling converters in this manner has the added benefits of reducing the input filter stress, distributing the converter thermal load, reducing volume and weight and many other advantages. Figure 1 is a typical example of a 3-phase current sharing group. Multiple current sharing groups and power rails can communicate and connect to the same DDC bus.

DDC bus

Zilker Labs (Digital-DC) products utilize a unique dedicated serial bus (DDC bus) to synchronize and communicate real-time events to other Zilker Labs devices connected to the Bus. A 5-bit address is assigned to each DDC rail, yielding a theoretical total of 32 separate power rails, including current sharing rails. Each device within a current sharing rail is assigned the same DDC address so the total number of DDC devices can exceed 32. A maximum of 8 devices or phases is allowed in a sharing group. Please ensure that the DDC signal integrity is maintained when using a large device count.

During DDC events, all devices will receive transmissions; however, only those devices configured to respond will do so. DDC devices can also transmit events if their programmed algorithm requires inter device communication. Some examples include fault spreading, sequencing, phase add/drop, broadcast margin and broadcast enable.

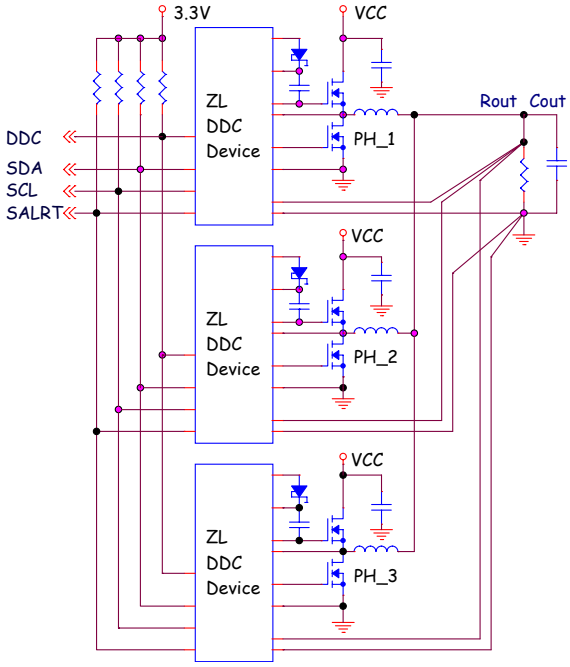

FIGURE 1. TYPICAL CURRENT SHARE APPLICATION

Active Droop Current Sharing

Zilker Labs current sharing devices use a patented form of digitally controlled active droop, resulting in the highest degree of phase current balancing.

Reference Device

The specific droop is configured based on the application and is set to the same value for each group member. The ZL device with the lowest sharing group position (specified in the ISHARE_CONFIG command, see page 9) is designated as the Reference Device. The Reference Device continuously broadcasts its inductor current over the DDC bus, while each Member device receives the transmission and trims its output voltage up or down until all group members supply the same current to the load. The process of broadcasting the Reference's load current and trimming each Member's output voltage to achieve current balance continues unless a fault occurs or a phase is dropped.

Current Sharing Algorithm

Figure 2 is an example of a current sharing application whose loadlines were all configured to 1mΩ. Due to differences in layout and IC production variances the actual member loadlines contain slope differences; they are exaggerated in this example.

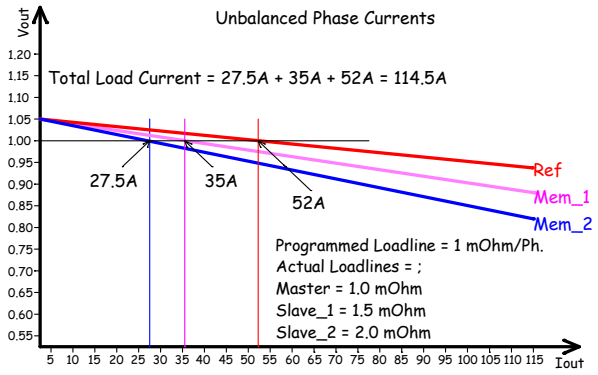

FIGURE 2. UNBALANCED PHASE CURRENTS DUE TO SLOPE ERROR

The minor imbalance results in each phase contributing an unequal portion of the load current. The imbalance is detected as the Reference's load current is broadcast and each Members reference voltage is trimmed up or down until all devices in the group carry an equal portion of the load current. This effect is shown in Figure 3. Notice in this case the Reference initially sourced the majority of the load current. Each member device's reference voltage was trimmed in the positive direction until all phase's source equal current to the load.

The recommended droop or loadline resistance for current sharing groups is between 0.5mΩ's and 1.5mΩ's. Each group member is assigned the same droop value. The equivalent droop is adjusted to the value entered as the individual member droop. This value of droop is maintained even when device(s) are added or dropped.

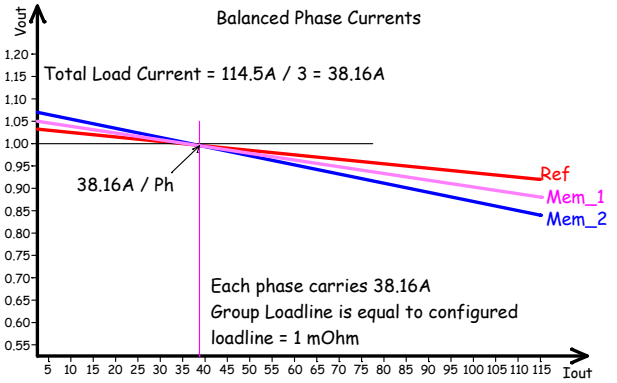

FIGURE 3. MEMBER(S) REFERENCE VOLTAGE IS TRIMMED UNTIL ALL DEVICE CURRENTS EQUALIZE

Current sharing equilibrium is shown in Figure 4 with a singular loadline being plotted that represents the actual static response for the sharing group. Since each group member in this example is configured to 1mΩ, the slope of the sharing group is equal to 1mΩ.

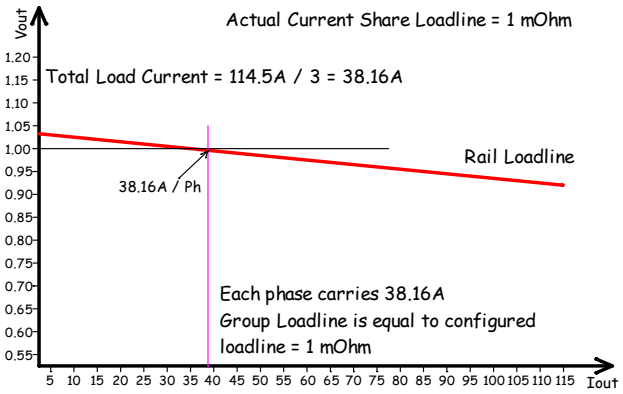

FIGURE 4. CURRENT SHARING PHASE BALANCE IS ACHIEVED.

Phase Add / Drop

When Zilker Labs Digital-DC power conversion devices are configured in a current sharing group, individual group members are capable of (dynamically) dropping out and adding back to the group. Group members are typically dropped or added to improve efficiency or to process a fault.

Group members can be added or dropped on the fly using a separate power management host controller invoking the Phase Control command, or by using the GUI.

Dropped Phase / SYNC CLOCK

If the dropped group member was supplying the SYNC clock, it will continue to do so even though it has become inactive. If the device supplying the SYNC clock dropped from the group and is no longer capable of supplying the clock, the remaining members will detect the absence of SYNC and respond according to their fault spreading configuration. If a host or power system manager is monitoring the group, then SALRT will assert, and the PMBus can be read and will respond with the appropriate fault management alarm as described in the PMBus Power System Mgt Protocol Specification – Part II.

If the dropped phase was the group reference, a new reference will be reassigned based on the lowest Phase Position number of the existing operational members. However, if the dropped reference was supplying the SYNC clock it will continue to do so. The phase position is defined by the angular offset relative to the SYNC clock and will autonomously redistribute based on the standing phases.

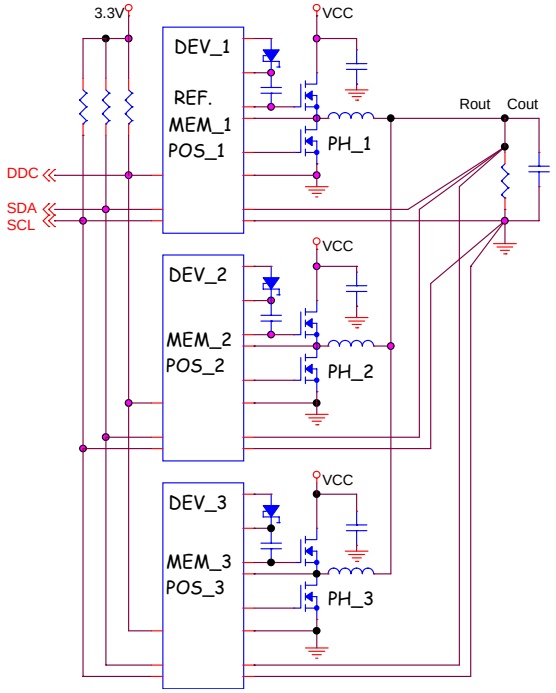

FIGURE 5. 3-PHASE CONVERTER SHOWING REFERENCE, MEMBER, AND POSITION NUMBER.

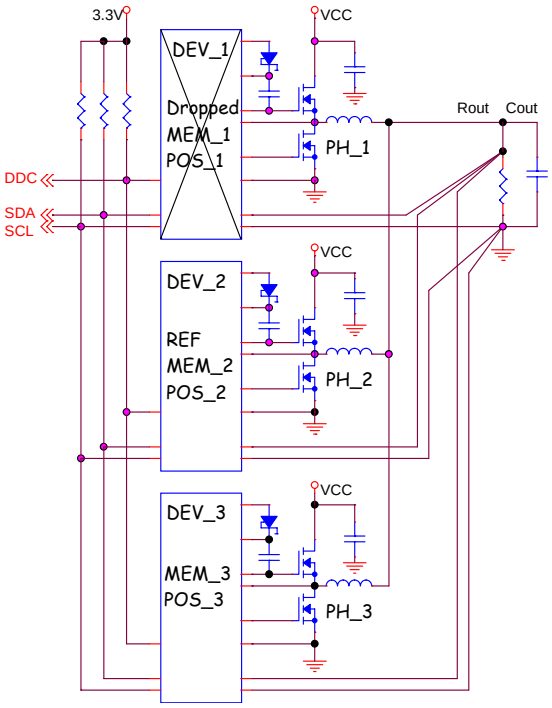

FIGURE 6. 3-PHASE CONVERTER AFTER REFERENCE PHASE IS DROPPED.

Figure 5 shows an example of a functional 3-phase current sharing group prior to asserting a Phase Control command to drop the reference phase (Device_1).

Figure 6 illustrates the new 2-phase configuration after the reference phase is dropped. Device_2 becomes the new reference for current sharing. Device_1 supplying the SYNC clock continues to do so.

The timing diagram is shown in Figure 7. After the reference phase is dropped the remaining two members are redistributed and the phase displacement changes from 120° to 180°.

Phase Add

The phase that was previously dropped may be added back into the group as determined by the power management host or the Phase Control command in the GUI. When the command is given to add the phase, the event is coordinated with the active member devices over the DDC bus, and the previously inactive device is seamlessly added back into the group. In this example, position 1 was made active and resumed the role of reference device, see Figure 5. The phase offset of each member was automatically redistributed from 180° to 120° as shown in the top section of Figure 7

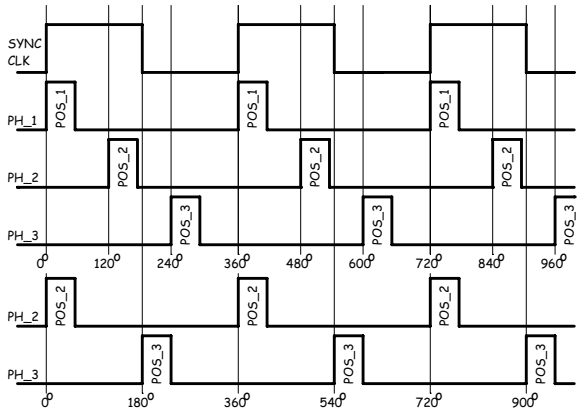

FIGURE 7. 3-PHASE CONVERTER TIMING DIAGRAM BEFORE AND AFTER PHASE_1 (REFERENCE PHASE) IS DROPPED.

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NLR Threshold Scaling

When multiple devices are configured in a current sharing group, the effective output ripple is divided by the number of active members. When all members of the group are operating, the NLR (Non Linear Response) thresholds can be set to a small value just above the minimum ripple amplitude. When a group member is dropped the ripple amplitude will increase.

In order to avoid spurious NLR activity the Digital-DC features automatically adjust the NLR thresholds

according to the ratio of *active* group members to *total* members of the group (see Equation 1).

$$Vt\_part = Vt\_all * \frac{Nall}{Nactive} \quad \text{(EQ. 1)}$$

Where

Vt_part is the NLR inner threshold setting used with some group members deactivated

Vt_all is the NLR inner threshold setting configured for the group with all members operating

Nall is the total number of members in the group

Nactive is the number of members active in the group (that is, the number of members not faulted or intentionally deactivated).

Nall and *Nactive* are determined automatically from the group configuration parameters. No additional programming or configuration is required.

Since the available thresholds are quantized to multiples of 0.5% of the configured output voltage, the next higher available threshold is used if the result of the above formula is fractional. For additional information about NLR, please reference AN2032 NLR Configuration DDC Products.

Automatic Phase Distribution

Digital-DC devices configured in current sharing groups feature the ability to autonomously perform phase offset. The offset resolution is 22.5° relative to the leading edge of the SYNC clock.

SYNC Clock

To configure a current sharing group, a common SYNC clock must be provided to each group member. This SYNC clock can be provided by any Zilker Labs Digital DC device, or the SYNC can be provided by an external source that satisfies the electrical specifications of the SYNC pin. **Note**: the switching frequency of each member must be configured to the same value.

Once the SYNC source has been designated, the SYNC pins of all group members and any other Zilker Labs device requiring synchronization and interleaving must be connected together as shown in Figure 8. Note that any of the devices whose SYNC pins are physically connected together can be configured to output the SYNC clock. The SYNC output can be configured as push-pull or open-drain. All other devices connected to the SYNC source must be configured as SYNC inputs.

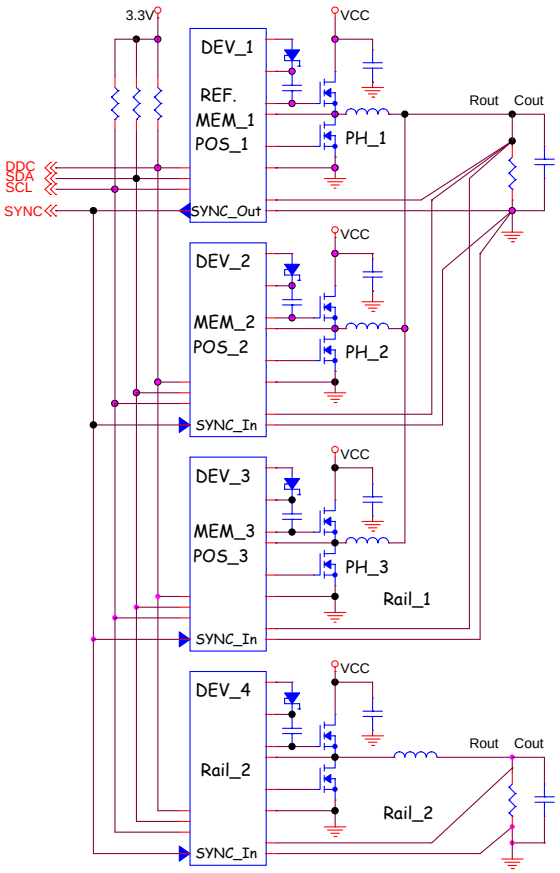

FIGURE 8. EXAMPLE OF SHARING GROUP AND AUXILIARY OUTPUT RAIL WITH A COMMON SYNC CLOCK.

Phase Offset

The current sharing group in Figure 8 will autonomously distribute each member's phase with respect to the SYNC clock. Since the sharing group contains 3 members, each member will be ideally offset in phase by 120°. The actual phase offset is represented by a 4 bit binary number resulting in 16 possible offset values in 22.5° steps. The real phase displacement will be rounded to the closest 22.5° increment. All possible phase displacements are shown in Figure 9.

For the 3-phase example shown in Figure 8. the actual sharing group phase offset will be rounded as shown in Table 1.

Although Rail_2 is connected to the same SYNC clock, it will not be autonomously offset in phase with respect to the current sharing group. Rail_2 can be offset in phase to one of the 16 possible offset values by using the INTERLEAVE command. If the INTERLEAVE command is not used, Rail_2 will simply turn on at 0° with the rising edge of the SYNC clock.

TABLE 1. IDEAL VS ACTUAL PHASE OFFSET

	IDEAL OFFSET	ACTUAL OFFSET
Position_1	0°	0°
Position_2	120°	112.5°
Position_3	240°	247.5°

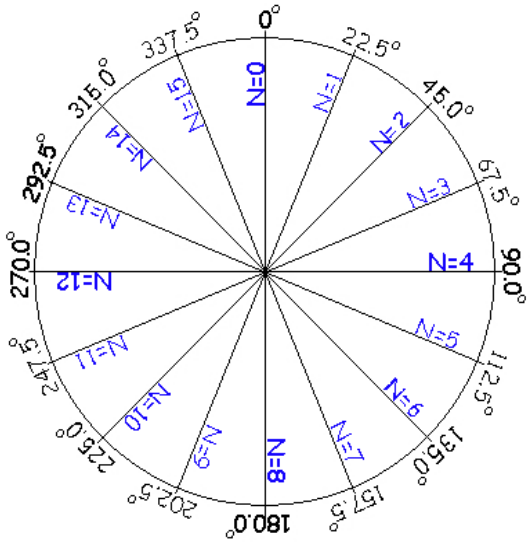

FIGURE 9. PHASE OFFSET RESOLUTION WHEEL

INTERLEAVE Command

Current sharing groups are autonomously offset in phase with respect to each group member, however when there are multiple sharing groups connected to the same SYNC clock the 2 groups will not autonomously offset from each other. Consider the 2 current sharing groups shown in Figure 10. This configuration consists of 2 output rails with each rail containing a 2-phase sharing group and a common SYNC clock.

Each sharing group will autonomously phase spread within the group, but not between the 2 groups. The resulting timing waveform is shown in Figure 11.

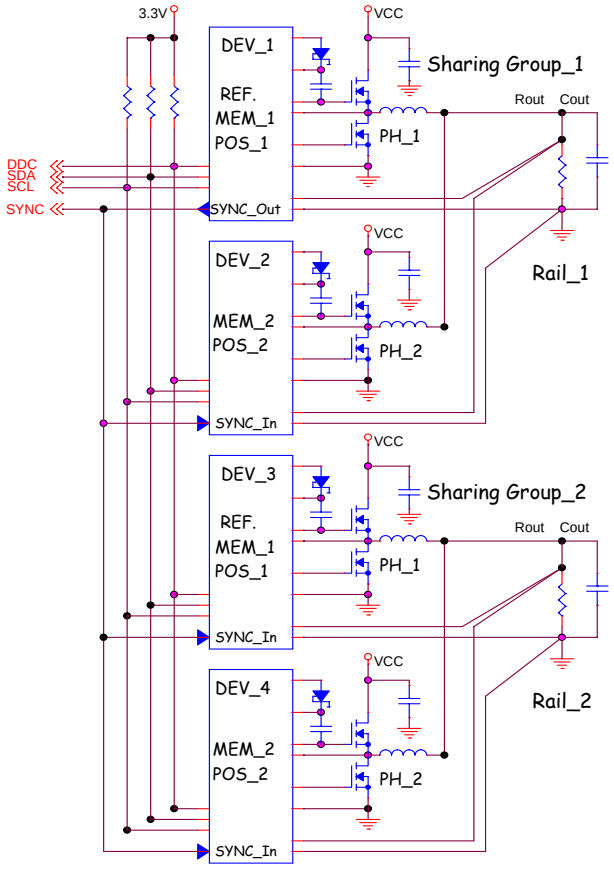

FIGURE 10. EXAMPLE OF 2 X 2-PHASE CURRENT SHARING GROUPS USING THE SAME SYNC CLOCK

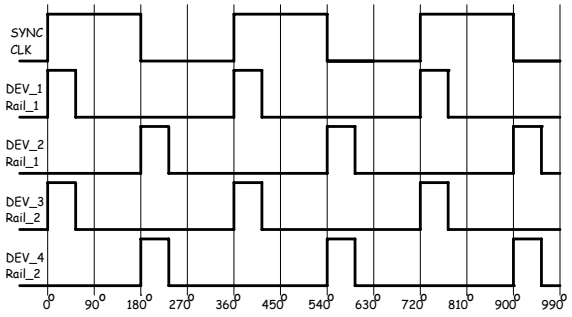

FIGURE 11. TIMING DIAGRAM FOR A 2 RAIL x 2-PHASE CURRENT SHARING EXAMPLE

Notice that the positional phase equivalents in each sharing group are not offset from each other.

If desired, Sharing Group_2 can be offset in phase from Group_1 by using the INTERLEAVE command field in the GUI or creating an equivalent command line in a configuration file.

The simplest way to achieve equal phase offset for the 4 devices in Figure 10 is to offset Sharing Group_2 by 90°. This is easily done in the GUI by declaring 2 Devices in Sharing Group_2 and assigning the Position in Interleave Group as 4.

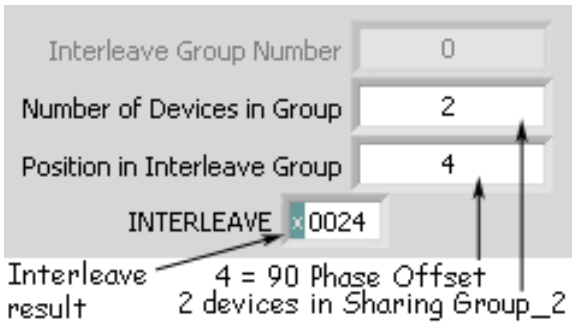

FIGURE 12. INTERLEAVE CONFIGURATION TO OFFSET SHARING GROUP_2 BY 90°

Referencing Figure 9, the value 4 represents an offset of 90°. The same entries are made for both devices in Sharing Group_2.

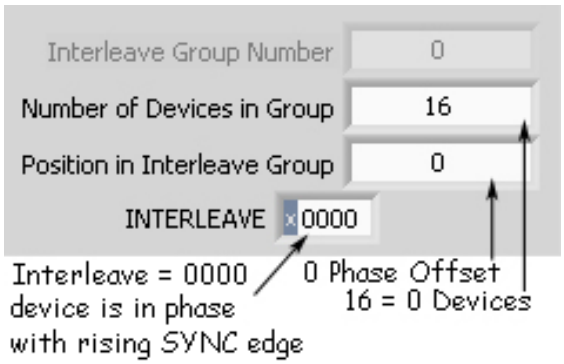

FIGURE 13. INTERLEAVE CONFIGURATION FOR 0 OFFSET (AUTONOMOUS PHASE CONTROL)

The interleave value for Sharing Group_1 is simply INTERLEAVE = 0000. Each respective hex INTERLEAVE value can be entered into a configuration file.

The new timing diagram shown in Figure 14 illustrates that each 2-phase sharing group is now equally offset in phase.

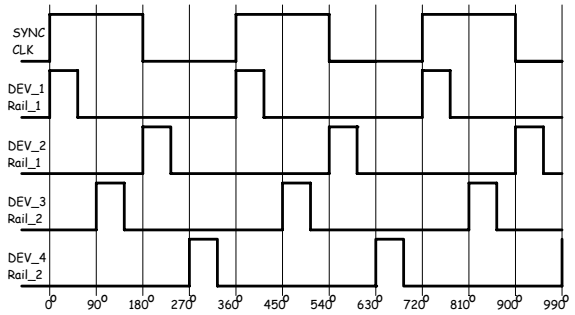

FIGURE 14. 2 X 2-PHASE CURRENT SHARING GROUPS NOW EQUALLY OFFSET USING INTERLEAVE COMMAND.

Ramp Synchronization

During turn-on and turn-off, the voltage ramps of each phase are synchronized to start at the same time. This ensures that inter-phase circulating currents are minimized.

Each current sharing phase contains a separate digital controller that executes firmware. The individual controller firmware requires synchronization prior to ramp events to minimize circulating currents.

This is accomplished by forcing the reference phase to wait at least one additional firmware cycle during ramping events by configuring it to have additional Time On and Time Off Delay relative to the other group members.

When the sharing group receives a hardware or PMBus enable, the member devices initialize their registers and freeze the state of their firmware, once the reference phase completes its extra timing delay it transmits a DDC Ramp Flag and all members of the group produce a sequenced PWM and begin their soft-start routine.

FIGURE 15. START-UP SYNCHRONIZATION

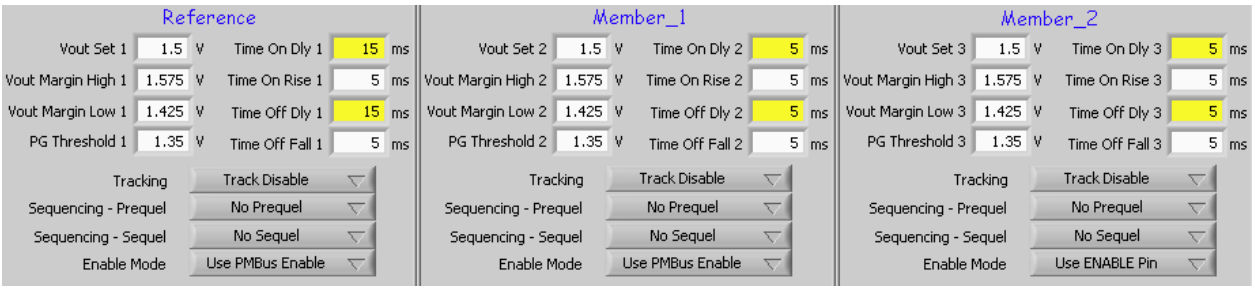

FIGURE 16. SETTING THE REFERENCE TIME ON/OFF DELAYS 10ms GREATER THAN MEMBER DELAYS

Please ensure that the Time On Delay and Time Off Delay parameters for the reference phase are at least 10ms greater than the delay parameters of each member device as shown in Figure 16.

Alternate Ramp Control

Alternate Ramp Control is used to avoid regulation at ground as the current share members are enabled and waiting for the Reference Phase to cycle through an extra firmware loop. Once the Reference phase is ready, it transmits a DDC ramp flag and all of the current share phases produce a turn-on rise time profile as shown in Figure 17.

The Set Alternate Ramp control is located in the MFR_CONFIG field on the PMBus Advanced page of the GUI.

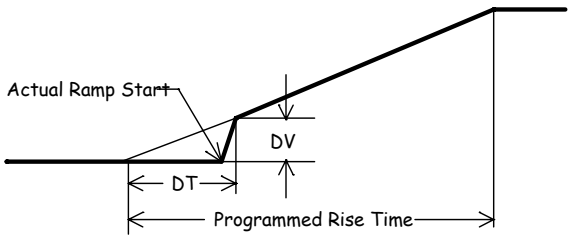

FIGURE 17. EFFECT OF SETTING ALTERNATE RAMP

Alternate Ramp

Setting Alternate Ramp control to enable produces a clean dual slope monotonic output voltage ramp at turn-on. The actual programmed rise time is conserved as shown in Figure 17. Alternate ramp must be set to enable for current sharing groups.

Minimum Duty Cycle

Current sharing groups can be comprised of 2 to 8 phases. Each phase contains its own digital PID controller.

To ensure that each controller produces an identical pulse width at start-up the Min Duty Cycle command must be set to enable. This starts each sharing group member with the same initial pulse width.

The Min Duty Cycle command is located in the USER_CONFIG field on the PMBus Advanced section of the GUI. The default value of the minimum duty cycle is $F_{SW}/128$.

Broadcast Enable / Margin

PMBus enable and margining commands can be configured with current sharing groups just like single phase converters. All devices must be connected to the same SMBus and DDCBus. The broadcast group can be comprised of current sharing devices and Single Phase devices. An example is shown in Figure 18. This configuration contains 3 Single Phase converters (Rails_1-3) and a 3-phase current sharing group (Rail_4).

To configure a current sharing broadcast group assign each group member the same Rail DDC ID. Assign the same Broadcast Group Number to all devices that will respond to the broadcast command. These assignments are shown in Table 2.

TABLE 2. ASSIGNING BROADCAST PARAMETERS

DEVICE	RAIL #	RAIL DDC ID	BROADCAST GROUP	BROADCAST ENABLE	BROADCAST MARGIN
1	1	1	2	ENABLE	ENABLE
2	2	2	2	ENABLE	ENABLE
3	3	3	2	ENABLE	ENABLE
4	4	5	2	ENABLE	ENABLE
5	4	5	2	ENABLE	ENABLE
6	4	5	2	ENABLE	ENABLE

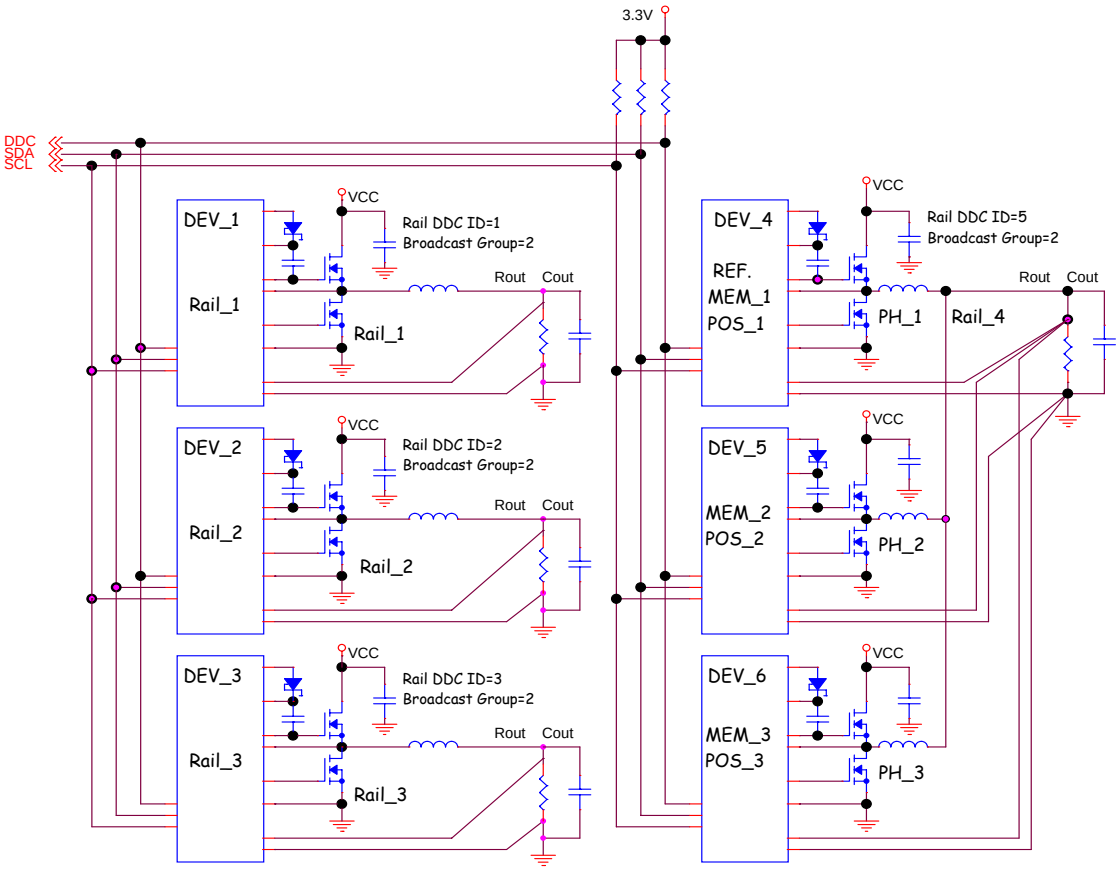

FIGURE 18. 4-RAIL POWER SUPPLY WITH PMBUS BROADCAST MARGIN AND ENABLE

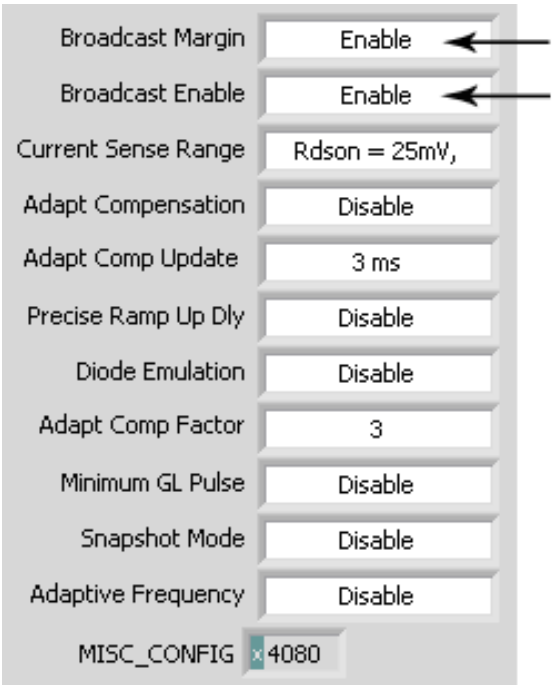

FIGURE 19. SETTING BROADCAST ENABLE AND MARGIN IN THE MISC_CONFIG FIELD

The DDC_CONFIG GUI entries for this example are shown below in Figure 20. After the Rail DDC ID and Broadcast Group are assigned the Broadcast Enable and/or Broadcast margin command(s) must be enabled in the MISC_CONFIG section of the GUI shown in Figure 19.

To use Broadcast Margin, enable the output rail(s) under test using PMBus Enable of any broadcast member or configure the rail(s) to use hardware enable. Once the rail(s) are enabled use the GUI to select the appropriate margining command located on the front page of the GUI see Figure 21. Use the Configure Device page of the GUI to change the margining range. The default range is automatically calculated to be ±5% of the nominal output voltage. Verify that all current share members have the same margin settings.

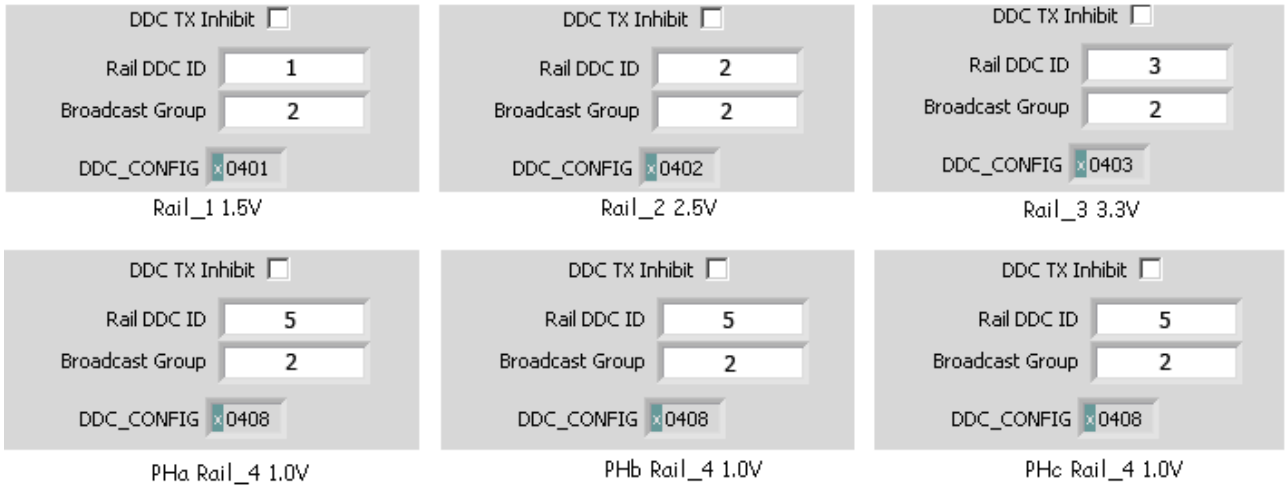

FIGURE 20. DDC_CONFIG GUI TO ENABLE BROADCAST ENABLE AND MARGIN

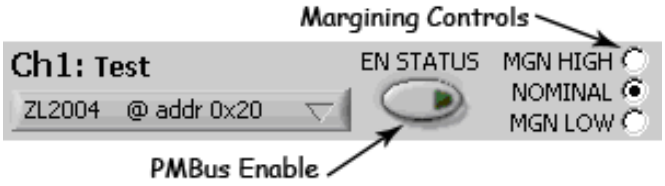

FIGURE 21. PMBUS ENABLE AND MARGIN CONTROL LOCATED ON GROUP PAGE OF THE GUI

Configuring Current Sharing

Consider the 3-phase current sharing group shown in Figure 22. Ensure that each Zilker Labs device in the group is connected to the same DDC and SMBus. The device with the lowest Device Position becomes the initial Reference Phase. The Reference phase is used to provide the load current information to each member device. If the Reference Device is dropped or faults the device with the next lowest Device Position becomes the new Reference Device.

1. (DDC_CONFIG)

Assign the same Rail DDC ID to each device in the current sharing group. If there are other non-current sharing devices connected to the same DDC bus make sure that those output rails have a unique Rail DDC ID. In this example, the Rail DDC ID = 5 for each current sharing devices.

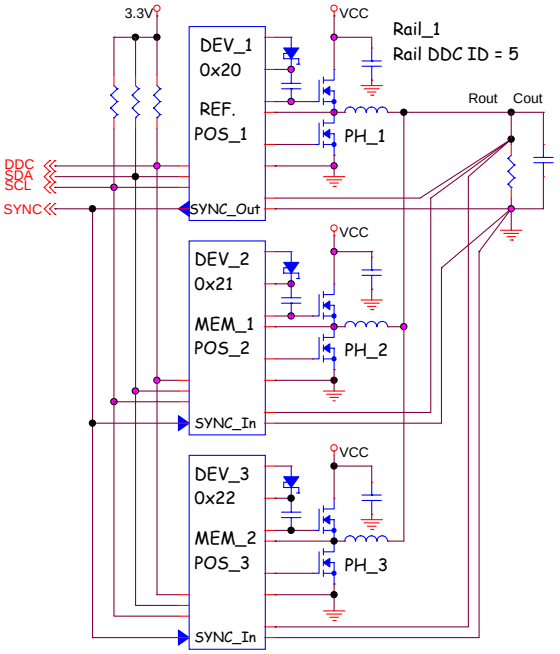

FIGURE 22. 3-PHASE CURRENT SHARING EXAMPLE

2. (ISHARE_CONFIG)

The ISHARE_CONFIG field contains the three entries:

a. Number of Devices = number of devices or phases in current sharing group

b. Device Position = Autonomous interleave position relative to SYNC Clock

c. Current Share Control = Enables current sharing

For this example the specific entries for each address is shown in Table 3 on page 10.

TABLE 3. ISHARE_CONFIG CURRENT SHARE VALUES

PHASE	SMB_{US} ADDRESS	NO. OF DEVICES	DEVICE POSITION	CURRENT SHARE CONTROL
Reference	0x20	3	1	Enabled
Member 1	0x21	3	2	Enabled
Member 2	0x22	3	3	Enabled

The GUI entries are shown in Figure 23.

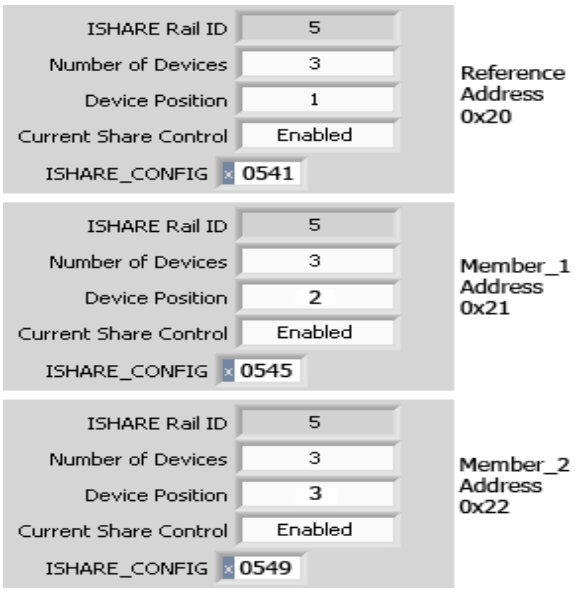

FIGURE 23. ISHARE_CONFIG GUI VALUES

3. (USER_CONFIG)

The following parameters located in the USER_CONFIG field (see Figures 24 and 25) on the PMBus: Advanced page pertain to current sharing groups and must be set to properly configure current sharing.

a. Min Duty Cycle

The minimum allowable duty cycle must be set to Enable to ensure that each phase starts the turn-on ramp with the same pulse width. Enabling Min Duty Cycle sets the default minimum value to $F_{SW/128}$.

b. SYNC Time-out Enable

SYNC always on if the device is providing the SYNC source. Typically the Reference Device is used to provide the SYNC Clock. However any device internal or external to the sharing group can provide the SYNC Clock.

For Member devices the SYNC Time-out Enable parameter can be set to SYNC off in 500ms. This will save a little power by shutting down the SYNC clock 500ms after Enable is deasserted.

c. SYNC Input Mode/SYNC Pin Configuration

The SYNC Input Mode is used along with the SYNC Pin Configure parameter to specify whether the device will output the SYNC clock or use the SYNC clock as an input.

SYNC Clock Source mode: set SYNC Input Mode to Pinstrap Input and set SYNC Pin Configure to Output Int. Signal. The DDC device will now operate as a clock source. Configure the SYNC Output Mode command in the MFR_CONFIG field to be Push-Pull or Open Drain to satisfy your system design requirements. Reference the device data sheet for additional information.

SYNC CLOCK INPUT MODE:

Sync Pin Configure is used to assign the internal clock as an output or as an input.

Set the SYNC Pin Configure parameter to Input Only if the device is using the SYNC clock as an input.

d. Standby Mode

Standby mode must be set to Monitor Enabled for both Reference and Member Devices. Setting this parameter to monitor mode ensures that the firmware is initialized prior to enabling the output rail.

The other entries in the USER_CONFIG field do not affect current sharing groups, and should be configured to meet the designer's system requirements. For additional information about these parameters please reference AN26 Power Navigator Users Manual and AN33 Zilker Labs PMBus Command Set – DDC Products.

The **USER_CONFIG** GUI entries for this example are shown in Figure 24, illustrating the configuration for the Reference device. Figure 25 illustrates the configuration for Member device(s).

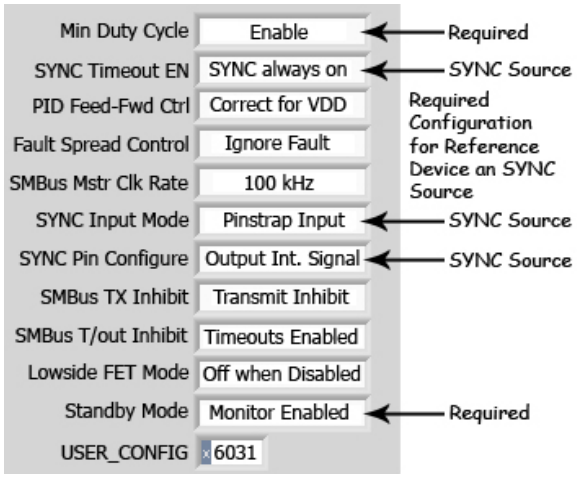

FIGURE 24. USER_CONFIG FIELD (REFERENCE)

Reference AN2026 *Power Navigator Users Manual* for additional information.

SMBUS TX INHIBIT

e. SMBus TX controls the Bus mastering capabilities of Zilker Labs products that don't use the DDCBus. SMBus TX Inhibit should be set to Transmit Inhibit for the DDCBus products referenced in this document.

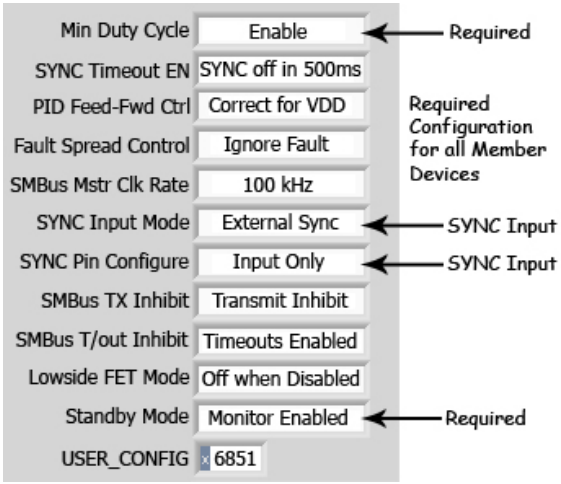

FIGURE 25. USER_CONFIG FIELD (MEMBER)

4. (MFR_CONFIG)

The following parameters located in the MFR_CONFIG field (see Figure 26) in the GUI PMBus: Advanced page must be set to properly configure current sharing.

a. I Sense Delay

The I Sense Delay parameter controls the blanking time between switching the top or bottom FET, allowing the filtering of noise associated with turning the switching devices on and off from the current measurement circuit. The actual value selected depends on F_{SW}, sensing method and duration of the resonant ring-out due to circuit parasitics. Ensure that the same blanking value is used for the Reference and Member device(s).

b. I Sense Control

I Sense Control is used to configure the current sensing method. Various modes of current sensing are available depending on duty cycle and switching frequency. Current sensing options are shown below in Table 4. A lumped or distributed resistor can be substituted for $r_{DS(ON)}$ and DCR sensing. Ensure that the same I Sense Control is used for the Reference and Member device(s).

TABLE 4. CURRENT SENSING METHOD SELECTION

CURRENT SENSE CONTROL	USAGE
Ground Referenced, down-slope ($r_{DS(ON)}$)	Low duty cycle and low F_{SW}
V_{OUT} Referenced, down-slope (Inductor DCR Sensing)	Low duty cycle and high F_{SW}
V_{OUT} Referenced, up-slope (Inductor DCR Sensing)	High Duty Cycle

c. NLR During Ramp

Determines if NLR is active during ramps or waits until Power Good is asserted. This should always be set to **Wait for PG** for both Reference and Member device(s) when configuring current sharing groups.

d. Alternate Ramp Control

Set to enable for Reference and Member device(s). Reference Alternate Ramp control in this document.

e. SYNC Output Mode

Configures the SYNC pin as Open Drain or Push-Pull. SYNC Output Mode is typically set to Push-Pull for the SYNC clock source and Open Drain for devices that receive the SYNC clock as an input.

The MFR_CONFIG GUI entries are shown below for this example. The comments refer to current sharing groups. Reference AN2026 *Power Navigator Users Guide* for additional information.

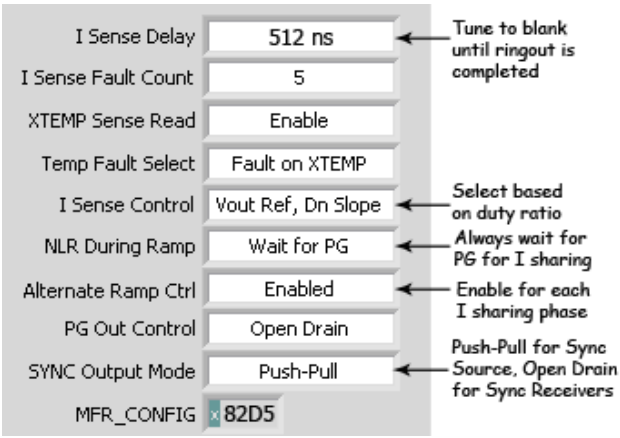

FIGURE 26. MFR_CONFIG FIELD

5. (TEMPCO_CONFIG)

The TEMPCO_CONFIG command is used to configure the temperature correction factor and temperature measurement source (internal or external) when performing temperature coefficient correction for the current sensing element. TEMPCO_CONFIG values are applied as a negative correction to a positive temperature coefficient. In general, the TEMPCO_CONFIG command is defined in Table 5.

TABLE 5. TEMPO_CONFIG

FIELD	PURPOSE	VALUE	DESCRIPTION
7	Selects the temperature sensor source for tempco correction	0	Selects the internal temperature sensor
		1	Selects the XTEMP pin for temperature measurements
6:0	Sets Tempco correction in units of 100ppm/°C	TC	$R_{SEN(EXT)}$
			$R_{SEN(INT)}$

Equation 2 can be used to fine tune the temperature correction for internal and external sense elements.

$$R_{SEN(EXT)} = IOUT\_CAL\_GAIN \times (1 + TC \times 10^{-4} \times (T - 25))$$
$$R_{SEN(INT)} = IOUT\_CAL\_OFFSET \times (1 + TC \times 10^{-4} \times (T - 25)) \quad \text{(EQ. 2)}$$

Where,

IOUT_CAL_GAIN = is the impedance of the current sense element at +25°C

IOUT_CAL_OFFSET = offset added to IOUT readings, this offset is used to compensate for current measurement error due to blanking.

TC = respective temperature coefficient

$R_{SEN(EXT)}$ = DCR inductor resistance

$R_{SEN(INT)}$ = internal silicon temp diode

$r_{DS(ON)}$ = low-side FET channel resistance

T = temperature measured by sensing device

TC = temperature correction factor

The hex values in Table 7 can be used to accurately compensate most designs if the measurement element is tightly (thermally) coupled to the sense element.

TABLE 6. TYPICAL TEMPCO_CONFIG VALUES BY ZL PART NUMBER

ZL DEVICE	EXTERNAL TEMP DIODE	INTERNAL SILICON DIODE
ZL2004	A8	2C
ZL2006	A8	2C

PMBus Basic Commands

(VOUT_COMMAND)

Set each current sharing phase to the same output voltage value.

(VOUT_TRIM)

Typically set to 0 (default value) for each current sharing phase. The reference phase will always retain a zero value. Member phases will adjust the trim value until all phases carry equal load current. If an offset voltage is desirable to overcome the effects of droop use the VOUT_CAL_OFFSET command to add an offset. See "(VOUT_CAL_OFFSET)".

(VOUT_CAL_OFFSET)

The VOUT_CAL_OFFSET command is used to apply an offset voltage that can compensate for the load-line droop. While positive and negative offset values are valid a positive offset value is typically used with a magnitude of Equation 3.

$$VOUT\_CAL\_OFFSET = 0.5 \times I_{MAX} \times R_{DROOP} \quad \text{(EQ. 3)}$$

If the VOUT_CAL_OFFSET command is used ensure that each group member is assigned the same VOUT_CAL_OFFSET value.

(VOUT_DROOP)

Droop resistance is used as part of the current sharing algorithm. The recommended droop or loadline resistance for current sharing groups is between 0.5mΩ's and 1.5mΩ's. Each group member is assigned the same droop value.

(MAX_DUTY)

The maximum duty cycle must be constrained as the switching frequency increases. Configure the MAX_DUTY cycle to a maximum value for each group member per Equation 4, round the result down to the closest integer value. Table 7 lists MAX_DUTY values for a few common switching frequencies.

$$\delta \max(\%) = [1 - (150ns \times Fsw)] \times 100 \quad \text{(EQ. 4)}$$

TABLE 7. MAX_DUTY VALUES FOR COMMON SWITCHING FREQUENCIES

FSW (kHz)	MAX DUTY (%)
200	97
400	94
600	91
800	88
1000	85
1400	80

(TON_DELAY), (TOFF_DELAY)

Time On Delay and Time Off Delay parameters for the reference phase must be set at least 10ms greater than the delay parameters of each member device, reference Figure 16.

(DEADTIME)

Zilker Labs requires that the H-L and L-H deadtimes are both set to a maximum value of 56ns to obtain performance and reliability. The maximum deadtime values can be reduced in increments of 4ns if the worst case transition times are known. Hex 0x3838 configures both deadtime edges to a maximum of 56ns.

The deadtimes of both PWM edges will dynamically find the most efficient operating point between 56ns and the minimum value configured with the DEADTIME_CONFIG command. Please reference Figure 27.

The DEADTIME command must precede the DEADTIME_CONFIG command in the text based configuration file.

(DEADTIME_CONFIG)

Zilker Labs recommends that the Min Deadtime H-L and L-H are both set to a value of 16ns to obtain performance and reliability, if the minimum transition times are known to be less than 16ns this number can be reduced in

increments of 4ns. Hex 0x0808 configures both pwm edges as dynamic with a 16ns minimum deadtime. Please reference Figure 27.

The DEADTIME command must precede the DEADTIME_CONFIG command in the text based configuration file.

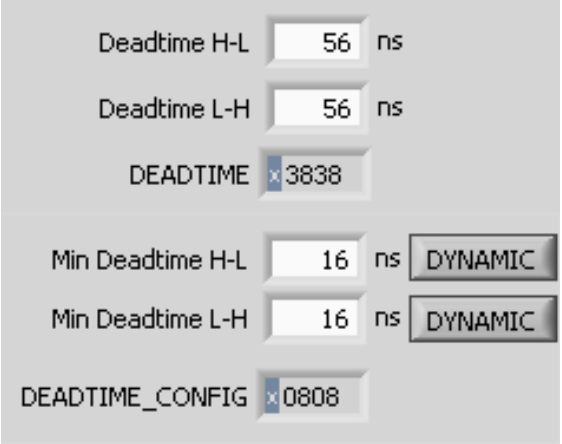

FIGURE 27. RECOMMENDED DEADTIME CONFIGURATION

Compensation

There are several ways and methods to approach compensating current sharing groups. Many of these methods require expensive equipment and advanced mathematical procedures. The compensation method presented here uses the Zilker Labs CompZL program to obtain PID taps that ensure stability and result in moderate to optimal transient response.

(Filter Design)

The design of the output filter is based on the system requirements for ripple, noise, transient response, and phase-count.

After the filter design is complete consider any one of the phases for the compensation analysis and divide the total capacitance by the number of phases. The resultant filter consists of the phase output inductor and the equivalent phase capacitance. Consider the 3-Phase example shown in Figure 28. This schematic is drawn symmetrically with identical phase filters; consider any one of the phases plus any common output capacitance divided by the number of phases, in this case 3.

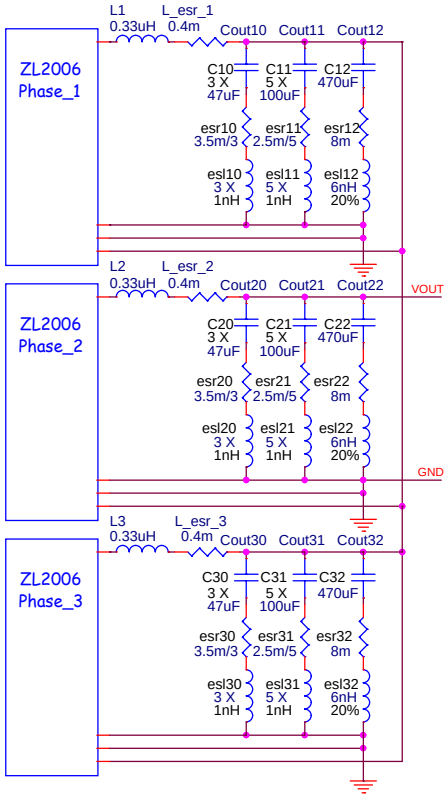

FIGURE 28. 3-PHASE CURRENT SHARING EXAMPLE

The resultant 3-Phase compensation model reduces to the configuration shown in Figure 29.

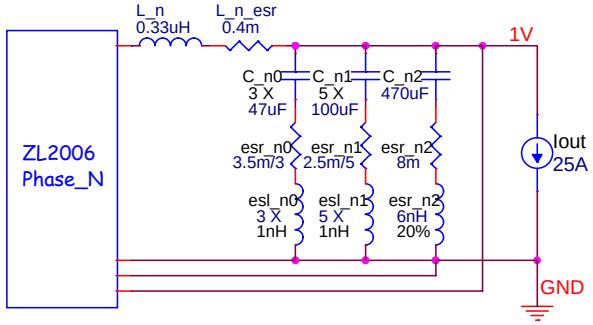

FIGURE 29. CURRENT SHARING COMPENSATION MODEL (USING COMPZL TO CALCULATE TAPS)

(Using CompAZL to Calculate Taps)

In order to calculate accurate taps for the sharing group, all of the conversion losses need to be identified and entered into the CompZL power stage model. These losses include inductor AC loss, routing loss, and FET switching loss.

It is particularly important to identify and estimate these losses with low impedance (hi Q) output filters. These previously unaccounted losses increase the filter damping and usually enable the use of real zeros in the compensator.

Real zeros can be strategically placed above and below the filter resonant frequency and result in increased midband frequency gain. Please reference AN35 for additional information on using CompZL.

Equations 5 to 11 can be used to estimate the conversion losses that are not included in CompZL, including these losses in the analysis increases circuit damping and the effectiveness of using real zeros. Once the analysis is complete, simply substitute the calculated value R_{DCR}' into the CompZL model for DCR.

R_{DCR}' is calculated by subtracting the losses known by CompZL from the total circuit losses. The total losses are known by measuring, calculating, or estimating the conversion efficiency at the operating point of interest. Once the efficiency is known, these equations (Equations 5 to 11) can be used to obtain the unaccounted losses at the operating point of interest.

$$R'_{DCR} = \frac{P_{IN} - P_{HI\_Cond} - P_{LO\_Cond} - P_{LOUT} - P_{OUT}}{I_{OUT}^2} \quad \text{(EQ. 5)}$$

$$P_{IN} = \left(\frac{P_{OUT}}{\eta} - V_{IN} * I_{QC} \right) \quad \text{(EQ. 6)}$$

$$P_{HI\_Cond} = I_{OUT}^2 * R_{DS\_HI} * \frac{V_{OUT}}{V_{IN}} \quad \text{(EQ. 7)}$$

$$P_{LO\_Cond} = \left(I_{OUT}^2 * R_{DS\_LO} \right) * \left(1 - \frac{V_{OUT}}{V_{IN}} \right) \quad \text{(EQ. 8)}$$

$$P_{LOUT} = I_{LOUT}^2 * R_{DCR} \quad \text{(EQ. 9)}$$

$$P_{OUT} = V_{OUT} * I_{OUT} \quad \text{(EQ. 10)}$$

$$I_{LOUT} = \sqrt{I_{OUT}^2 + \frac{\left[\frac{\left(1 - \frac{V_{OUT}}{V_{IN}} \right) \times V_{OUT}}{L_{OUT} \times F_{SW}} \right]^2}{12}} \quad \text{(EQ. 11)}$$

Where:

R_{DCR}' = Total resistive conversion loss minus CompZL calculated losses

P_{IN} = Total input power

P_{HI_Cond} = High-side FET Conduction loss

P_{LO_Cond} = Low-side FET Conduction loss

P_{LOUT} = Output inductor DCR loss

I_{OUT}^2 = Output current

R_{DS_LO} = Low-Side FET $r_{DS(ON)}$

R_{DS_HI} = High-Side FET $r_{DS(ON)}$

η = Converter efficiency

V_{IN} = Converter input voltage

V_{OUT} = Converter output voltage

I_{QC} = Controller quiescent current

I_{OUT} = Converter output current

I_{LOUT} = Output inductor RMS current

(Compensation Example)

The 3-Phase converter shown in Figure 29 has the following component values:

V_{OUT} = 1.0V

V_{IN} = 12V

I_{OUT} = 25A/Phase

F_{SW} = 615kHz/Phase

C_{OUT_n0} = 3 X 47µF, 3.5mΩ, 1nH

C_{OUT_n1} = 5 X 100µF, 2.5mΩ, 6nH

C_{OUT_n2} = 470µF, 8mΩ, 6nH

L_{OUT} = 0.33µH

DCR = 0.4mΩ

R_{DS_HI} = 4mΩ

R_{DS_LO} = 2mΩ

ç = 85%

I_{QC} = 35mA

The individual power losses are calculated in Equations 12 through 17. The losses already accounted for in CompZL are then subtracted from the input power.

$$P_{IN} = \left(\frac{1V * 25A}{0.84} - 12V * 35mA \right) = 28.99W \quad \text{(EQ. 12)}$$

$$P_{HI\_COND} = 25^2 A * 4m\Omega * \frac{1V}{12V} = 0.208W \quad \text{(EQ. 13)}$$

$$P_{LO\_COND} = 25^2 A * 2m\Omega * \left(1 - \frac{1V}{12V} \right) = 1.15W \quad \text{(EQ. 14)}$$

$$I_{LOUT} = \sqrt{25^2 A + \frac{\left[\frac{\left(1 - \frac{1V}{12V} \right) * 1V}{0.33uH * 615KHz} \right]^2}{12}} = 25.03A \quad \text{(EQ. 15)}$$

$$P_{LOUT} = 25.03^2 A * 0.4m\Omega = 0.25W \quad \text{(EQ. 16)}$$

$$P_{OUT} = 1V * 25A = 25W \quad \text{(EQ. 17)}$$

$$R'_{DCR} = \frac{29.34W - 0.204W - 1.145W - 0.25W - 25W}{25^2 A} = 3.82m\Omega \quad \text{(EQ. 18)}$$

The adjusted value of R'_{DCR} is 3.82mΩ. Type this value into the CompZL location for the inductor DCR. This adjusted value now contains all of the frequency dependent losses previously unaccounted for in the CompZL model.

This new adjusted value yields a more accurate compensation model and increases the filter dampening. As a result, the possibility of using real zeros increases with low impedance output filters.

(Suggested Guidelines)

To ensure that the digital PID controller constrains internal noise and minimizes PWM jitter, the low frequency gain Gc should be constrained to 30dB if possible. Q should be initially set between 0.1 to 0.4. The compensator should be set to Overdamped (real zeros). If the Q of the output filter is extremely low, (very small parasitic resistance) an overdamped compensator will not be possible.

The compensator natural frequency Fn is adjusted below the calculated output filter natural frequency (see Equation 19), by moving the zeros until the phase margin, gain margin, and crossover criteria is met.

The compensation results are shown in Figure 30. the compensator is set to overdamped (real zeros). The gain term was set to initially 25dB, and Q was set to 0.35.

$$Fn = \frac{1}{2 * \pi * \sqrt{Lout * Cout}} \quad \text{(EQ. 19)}$$

$$Fn = \frac{1}{2 * \pi * \sqrt{0.33uH * 1111uF}} = 8.31kHz$$

While moving each zero in turn, observe the actual phase and gain margin values and ensure that the phase and gain margin goals are met.

Notice how the gain levels off at approximately 2.5kHz. This is due to the careful placement of the zeros and results in a flattened midband gain characteristic with improved damping and transient response.

Once the PID coefficients have been calculated, enter the same values for each phase in their respective configuration files.

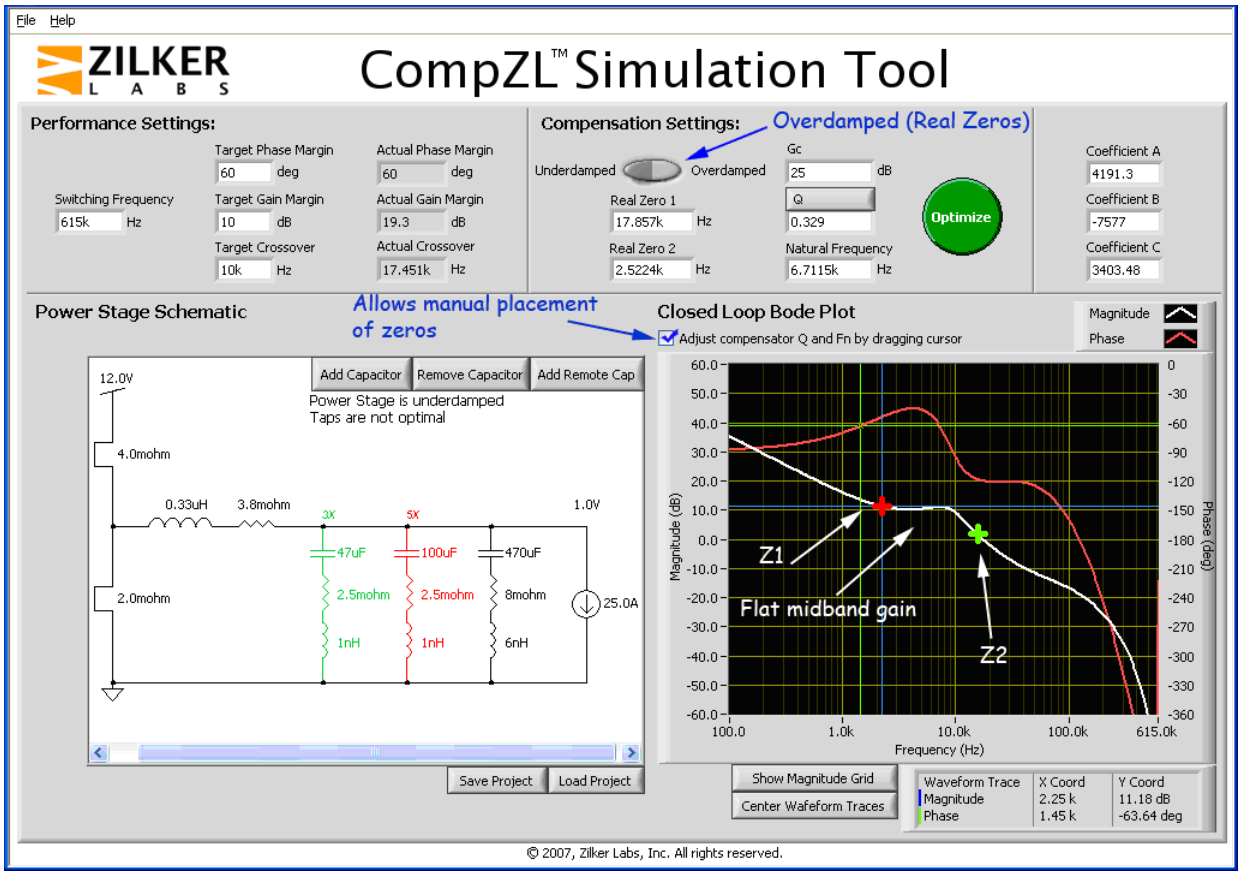

FIGURE 30. USING COMPZL IN THE MANUAL MODE

Configuration Files

Once the hardware design is completed and the design has been verified, a configuration file is created for each group member. The configuration file is composed or edited by using a text editor such as Microsoft Notepad. Other editors can be used as long as the filename has a .txt extension. The configuration file data can utilize both decimal and hexadecimal data. Hexadecimal data is always preceded by 0x. Comments can be added to the configuration file if preceded with a # sign.

Consider the 3-phase sharing group shown in Figure 31. The operating requirements are shown in Table 8.

Configuration files were composed for each phase and are shown in Figure 32. Reference AN2031 (Writing Configuration Files for Zilker Labs Devices) for additional information on composing configuration files.

See the “Configuration File Checklist” on page 17 to help establish recommended boundary conditions.

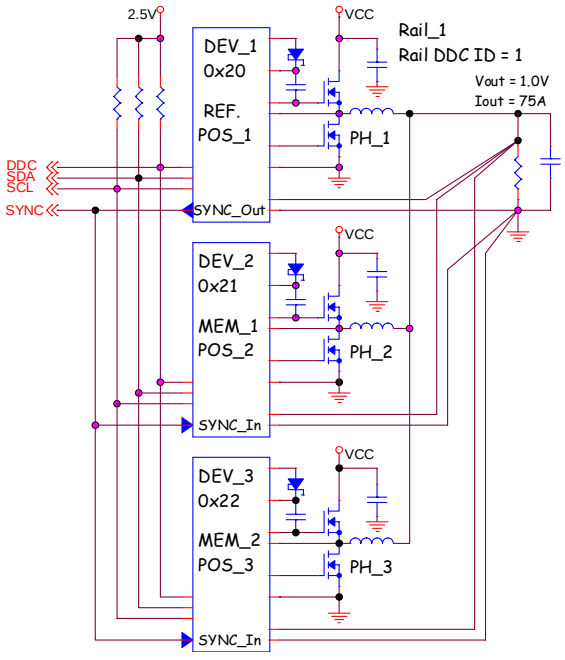

FIGURE 31. 3-PHASE SHARING GROUP EXAMPLE

TABLE 8. 3-PHASE SHARING GROUP REQUIREMENTS

DEVICE (PHASE)	ADDRESS (HEX)	SYNC	VIN (VOLTS)	V_{OUT} (AMPS)	I_{OUT} (AMPS)	F_{SW} (kHz)
PH_1Ref	0x20	Source	12	1.0V	25	615
PH_2Mem_1	0x21	Input	12	1.0V	25	615
PH_2Mem_2	0x22	Input	12	1.0V	25	615

Configuration File Checklist

Use the following checklist as a guideline when creating configuration files for current sharing rails.

1. Follow memory restore guidelines

- RESTORE_FACTORY
- STORE_USER_ALL
- STORE_DEFAULT_ALL
- RESTORE_DEFAULT_ALL
-
-
- STORE_DEFAULT_ALL
- RESTORE_DEFAULT_ALL

2. Assign the same VOUT_DROOP value to all ZL devices in the current sharing groupwith a value between 0.5Ω's and 1.5Ω's.
3. Ensure that the Time On Delay and Time Off Delay parameters for the reference phase are at least 10ms greater than the delay parameters of each member device, reference phases that contain telemetry data from the member device(s) I.E. ZL6102(3) require at least 15ms extra delay times for the reference device.
4. Assign the same fault responses for each device.
5. Designate and configure the SYNC source for the group, if the source is one of the group devices all other device(s) in the group are configured as SYNC inputs.
6. Assign the same DDC_RAIL_ID to each device in the group using DDC_CONFIG, except ZL6102(3) devices and derivatives. ZL6102(3) devices automatically assign their DDC Rail ID's based on their PMBus addresses. When using ZL6102(3)'s with other Zilker devices ensure that the DDC_Rail_ID's don't conflict.
7. Assign a unique phase position to each group device using ISHARE_CONFIG.
8. Enable Alternate Ramp Control for each group member.
9. Configure Standby Mode to Monitor Enabled for each group member.
10. Set the TEMPCO_CONFIG value for each group member to the same value.
11. Configure DEADTIME and DEADTIME_CONFIG commands with the DEADTIME command line always preceding DEADTIME_CONFIG. The recommended starting point is both edges set to DYNAMIC with a minimum deadtime of 16ns. The maximum deadtimes should be set to 56ns maximum.

- DEADTIME 0x3838
- DEADTIME_CONFIG 0x0808

12. Assign the maximum duty cycle to each group device per Equation 4.
13. Assign the same IOUT_CAL_GAIN to each group device in units of mΩ's.
14. Configure the Min Duty Cycle command to Enabled.
15. Configure SYNC Time-out EN to SYNC always On.
16. Diode Emulation, Adaptive Frequency Compensation is not supported with current sharing and must be disabled.
17. Continuous retries is not supported as a fault response for current sharing.

Reference (Phase_1)

Line Num.	Command	Value	Notes
1	RESTORE_FACTORY		#
2	STORE_USER_ALL		#
3	STORE_DEFAULT_ALL		# restores
4	RESTORE_DEFAULT_ALL		#
5	FREQUENCY_SWITCH	400	# kHz
6	ON_OFF_CONFIG	0x1A	# hardware enable
7	MFR_ID	Zilker Labs	
8	MFR_MODEL	ZL2006	
9	MFR_REVISION	EV2	
10	MFR_LOCATION	Austin	
11	MFR_DATE	10/29/08	
12	MFR_SERIAL		
13	VOUT_COMMAND	1.00	# volts
14	VOUT_MAX	1.15	# volts
15	VOUT_DROOP	1.00	# volts
16	VOUT_MARGIN_HIGH	1.05	# volts
17	VOUT_MARGIN_LOW	0.95	# volts
18	POWER_GOOD_ON	0.90	# volts
19	POWER_GOOD_DELAY	5	# ms
20	VOUT_OV_FAULT_LIMIT	1.15	# volts
21	VOUT_OV_FAULT_RESPONSE	0x80	# shutdown 0 delay
22	VOUT_UV_FAULT_LIMIT	0.85	# volts
23	VOUT_UV_FAULT_RESPONSE	0x80	# shutdown 0 delay
24	OVUV_CONFIG	0x80	# shutdown 0 delay
25	VIN_UV_WARN_LIMIT	10.8	# volts
26	VIN_UV_FAULT_LIMIT	9.600	# volts
27	VIN_UV_FAULT_RESPONSE	0x80	# shutdown 0 delay
28	VIN_OV_FAULT_LIMIT	14.40	# volts
29	VIN_OV_WARN_LIMIT	13.20	# volts
30	VIN_OV_FAULT_RESPONSE	0x80	# shutdown 0 delay
31	IOUT_SCALE	1.2	# Ω's
32	IOUT_CAL_OFFSET	-2	# amps
33	IOUT_OC_FAULT_LIMIT	67.50	# amps
34	IOUT_AVG_OC_FAULT_LIMIT	56.25	# amps
35	IOUT_UC_FAULT_LIMIT	-22.50	# amps
36	IOUT_AVG_UC_FAULT_LIMIT	-18.00	# amps
37	MFR_IOUT_OC_FAULT_RESPONSE	0x80	# shutdown 0 delay
38	MFR_IOUT_UC_FAULT_RESPONSE	0x80	# shutdown 0 delay
39	OT_WARN_LIMIT	110.0	# ^{O}C
40	OT_FAULT_LIMIT	120.0	# ^{O}C
41	OT_FAULT_RESPONSE	0x80	# shutdown 0 delay
42	UT_WARN_LIMIT	-20.0	# ^{O}C
43	UT_FAULT_LIMIT	-30.0	# ^{O}C
44	UT_FAULT_RESPONSE	0x80	# shutdown 0 delay
45	TON_DELAY	15	# ms
46	TON_RISE	5	# ms
47	TOFF_DELAY	15	# ms
48	TOFF_FALL	5	# ms
49	PID_TAPS		# pid coefficients
50	DEADTIME	0x3838	
51	DEADTIME_CONFIG	0x0808	
52	MAX_DUTY	94	# %
53	USER_CONFIG	0x6031	# sync source
54	MFR_CONFIG	0x82D5	
55	NLR_CONFIG	0x00000000	# disabled
56	MISC_CONFIG	0x4480	# broadcast enabled
57	DDC_CONFIG	0x0101	# ddc rail=1
58	ISHARE_CONFIG	0x0141	# current share en,pos_1
59	TEMPCO_CONFIG	0xA8	# ext.correction
60	STORE_DEFAULT_ALL		#
61	RESTORE_DEFAULT_ALL		# restores

Advanced Gui Entries

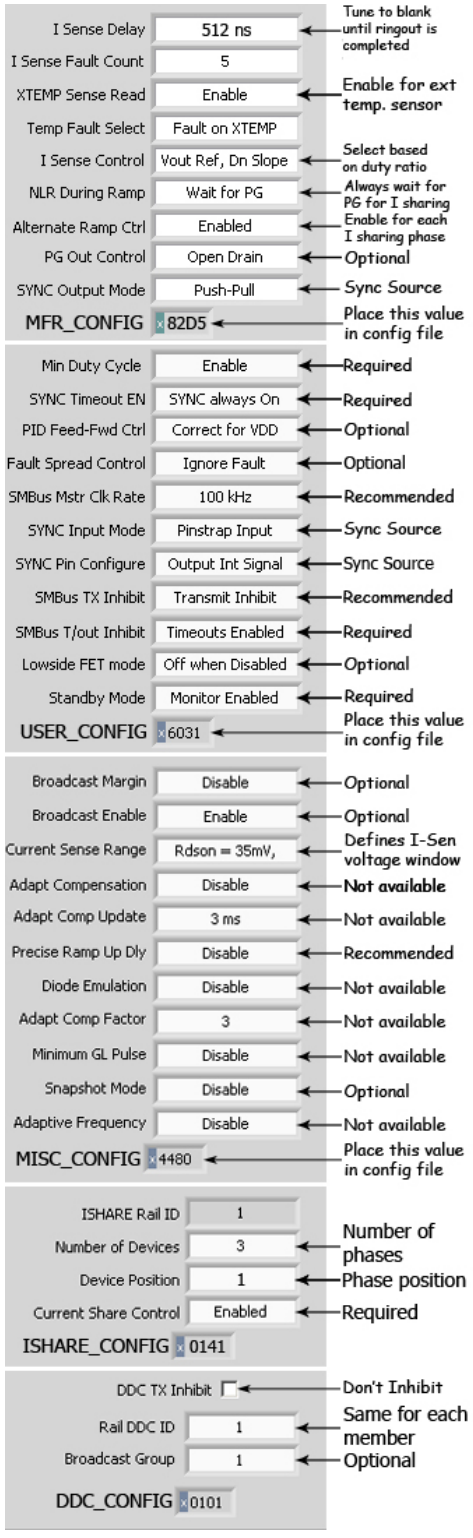

FIGURE 32. CONFIGURATION FILE FOR 3-PHASE CURRENT SHARING GROUP (REF_PHASE)

Member_1 (Phase_2)

Line Num.	Command	Value	Notes
1	RESTORE_FACTORY		#
2	STORE_USER_ALL		#
3	STORE_DEFAULT_ALL		# restores
4	RESTORE_DEFAULT_ALL		#
5	FREQUENCY_SWITCH	400	# kHz
6	ON_OFF_CONFIG	0x1A	# hardware enable
7	MFR_ID	Zilker Labs	
8	MFR_MODEL	ZL2006	
9	MFR_REVISION	EV2	
10	MFR_LOCATION	Austin	
11	MFR_DATE	10/29/08	
12	MFR_SERIAL		
13	VOUT_COMMAND	1.00	# volts
14	VOUT_MAX	1.15	# volts
15	VOUT_DROOP	1.00	# volts
16	VOUT_MARGIN_HIGH	1.05	# volts
17	VOUT_MARGIN_LOW	0.95	# volts
18	POWER_GOOD_ON	0.90	# volts
19	POWER_GOOD_DELAY	5	# ms
20	VOUT_OV_FAULT_LIMIT	1.15	# volts
21	VOUT_OV_FAULT_RESPONSE	0x80	# shutdown 0 delay
22	VOUT_UV_FAULT_LIMIT	0.85	# volts
23	VOUT_UV_FAULT_RESPONSE	0x80	# shutdown 0 delay
24	OVUV_CONFIG	0x80	# shutdown 0 delay
25	VIN_UV_WARN_LIMIT	10.8	# volts
26	VIN_UV_FAULT_LIMIT	9.600	# volts
27	VIN_UV_FAULT_RESPONSE	0x80	# shutdown 0 delay
28	VIN_OV_FAULT_LIMIT	14.40	# volts
29	VIN_OV_WARN_LIMIT	13.20	# volts
30	VIN_OV_FAULT_RESPONSE	0x80	# shutdown 0 delay
31	IOUT_SCALE	1.2	# Ω's
32	IOUT_CAL_OFFSET	-2	# amps
33	IOUT_OC_FAULT_LIMIT	67.50	# amps
34	IOUT_AVG_OC_FAULT_LIMIT	56.25	# amps
35	IOUT_UC_FAULT_LIMIT	-22.50	# amps
36	IOUT_AVG_UC_FAULT_LIMIT	-18.00	# amps
37	MFR_IOUT_OC_FAULT_RESPONSE	0x80	# shutdown 0 delay
38	MFR_IOUT_UC_FAULT_RESPONSE	0x80	# shutdown 0 delay
39	OT_WARN_LIMIT	110.0	# ^{O}C
40	OT_FAULT_LIMIT	120.0	# ^{O}C
41	OT_FAULT_RESPONSE	0x80	# shutdown 0 delay
42	UT_WARN_LIMIT	-20.0	# ^{O}C
43	UT_FAULT_LIMIT	-30.0	# ^{O}C
44	UT_FAULT_RESPONSE	0x80	# shutdown 0 delay
45	TON_DELAY	5.0	# ms
46	TON_RISE	5	# ms
47	TOFF_DELAY	5.0	# ms
48	TOFF_FALL	5	# ms
49	PID_TAPS		# pid coefficients
50	DEADTIME	0x3838	
51	DEADTIME_CONFIG	0x0808	
52	MAX_DUTY	94	# %
53	USER_CONFIG	0x6051	# sync input
54	MFR_CONFIG	0x82D4	
55	NLR_CONFIG	0x00000000	# disabled
56	MISC_CONFIG	0x4480	# broadcast enabled
57	DDC_CONFIG	0x0101	# ddc rail=1
58	ISHARE_CONFIG	0x0145	# current share en,pos_2
59	TEMPCO_CONFIG	0xA8	# ext.correction
60	STORE_DEFAULT_ALL		#
61	RESTORE_DEFAULT_ALL		# restores

Advanced Gui Entries

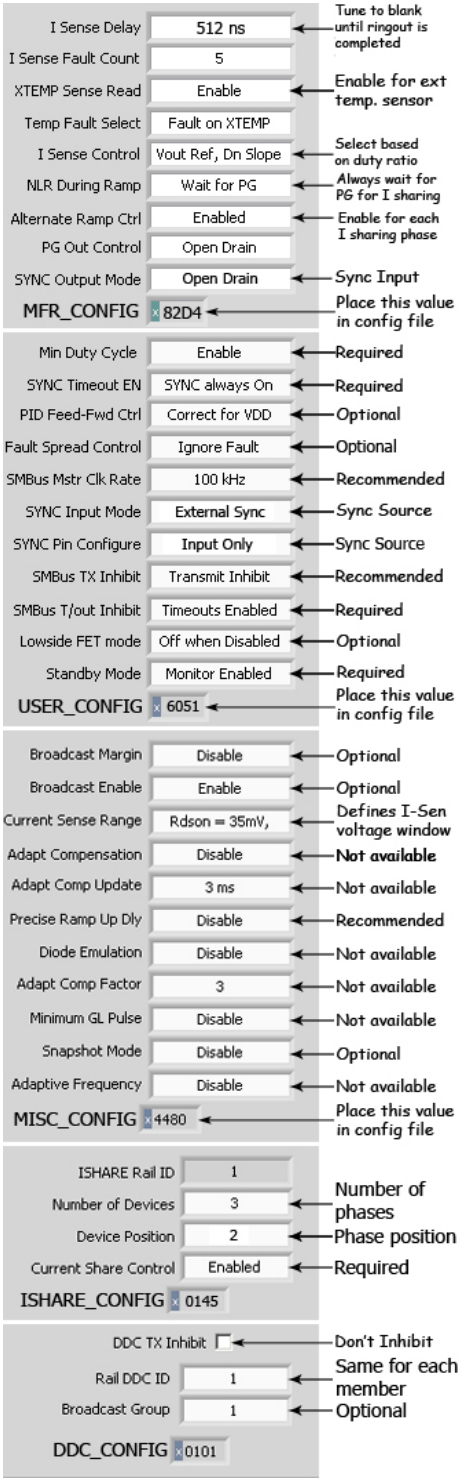

FIGURE 33. CONFIGURATION FILE FOR 3-PHASE CURRENT SHARING GROUP (MEM_1)

Member_2 (Phase_3)

Line Num.	Command	Value	Notes
			#
1	RESTORE_FACTORY		#
2	STORE_USER_ALL		# restores
3	STORE_DEFAULT_ALL		#
4	RESTORE_DEFAULT_ALL		#
5	FREQUENCY_SWITCH	400	# kHz
6	ON_OFF_CONFIG	0x1A	# hardware enable
7	MFR_ID	Zilker Labs	
8	MFR_MODEL	ZL2006	
9	MFR_REVISION	EV2	
10	MFR_LOCATION	Austin	
11	MFR_DATE	10/29/08	
12	MFR_SERIAL		
13	VOUT_COMMAND	1.00	# volts
14	VOUT_MAX	1.15	# volts
15	VOUT_DROOP	1.00	# volts
16	VOUT_MARGIN_HIGH	1.05	# volts
17	VOUT_MARGIN_LOW	0.95	# volts
18	POWER_GOOD_ON	0.90	# volts
19	POWER_GOOD_DELAY	5	# ms
20	VOUT_OV_FAULT_LIMIT	1.15	# volts
21	VOUT_OV_FAULT_RESPONSE	0x80	# shutdown 0 delay
22	VOUT_UV_FAULT_LIMIT	0.85	# volts
23	VOUT_UV_FAULT_RESPONSE	0x80	# shutdown 0 delay
24	OVUV_CONFIG	0x80	# shutdown 0 delay
25	VIN_UV_WARN_LIMIT	10.8	# volts
26	VIN_UV_FAULT_LIMIT	9.600	# volts
27	VIN_UV_FAULT_RESPONSE	0x80	# shutdown 0 delay
28	VIN_OV_FAULT_LIMIT	14.40	# volts
29	VIN_OV_WARN_LIMIT	13.20	# volts
30	VIN_OV_FAULT_RESPONSE	0x80	# shutdown 0 delay
31	IOUT_SCALE	1.2	# Ω's
32	IOUT_CAL_OFFSET	-2	# amps
33	IOUT_OC_FAULT_LIMIT	67.50	# amps
34	IOUT_AVG_OC_FAULT_LIMIT	56.25	# amps
35	IOUT_UC_FAULT_LIMIT	-22.50	# amps
36	IOUT_AVG_UC_FAULT_LIMIT	-18.00	# amps
37	MFR_IOUT_OC_FAULT_RESPONSE	0x80	# shutdown 0 delay
38	MFR_IOUT_UC_FAULT_RESPONSE	0x80	# shutdown 0 delay
39	OT_WARN_LIMIT	110.0	# ^{O}C
40	OT_FAULT_LIMIT	120.0	# ^{O}C
41	OT_FAULT_RESPONSE	0x80	# shutdown 0 delay
42	UT_WARN_LIMIT	-20.0	# ^{O}C
43	UT_FAULT_LIMIT	-30.0	# ^{O}C
44	UT_FAULT_RESPONSE	0x80	# shutdown 0 delay
45	TON_DELAY	5.0	# ms
46	TON_RISE	5	# ms
47	TOFF_DELAY	5.0	# ms
48	TOFF_FALL	5	# ms
49	PID_TAPS		# pid coefficients
50	DEADTIME	0x3838	
51	DEADTIME_CONFIG	0x0808	
52	MAX_DUTY	94	# %
53	USER_CONFIG	0x6051	# sync input
54	MFR_CONFIG	0x82D4	
55	NLR_CONFIG	0x00000000	# disabled
56	MISC_CONFIG	0x4480	# broadcast enabled
57	DDC_CONFIG	0x0101	# ddc rail=1
58	ISHARE_CONFIG	0x0149	# current share en,pos_3
59	TEMPCO_CONFIG	0xA8	# ext.correction
60	STORE_DEFAULT_ALL		# restores
61	RESTORE_DEFAULT_ALL		#

Advanced Gui Entries

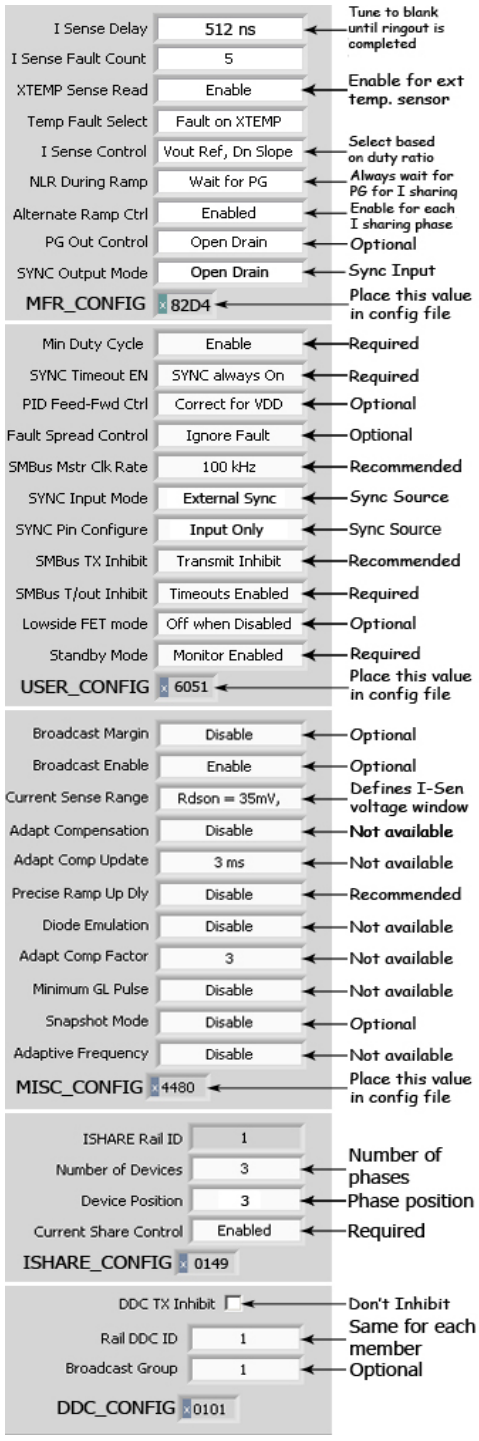

FIGURE 34. CONFIGURATION FILE FOR 3-PHASE CURRENT SHARING GROUP (MEM_2)

Notes